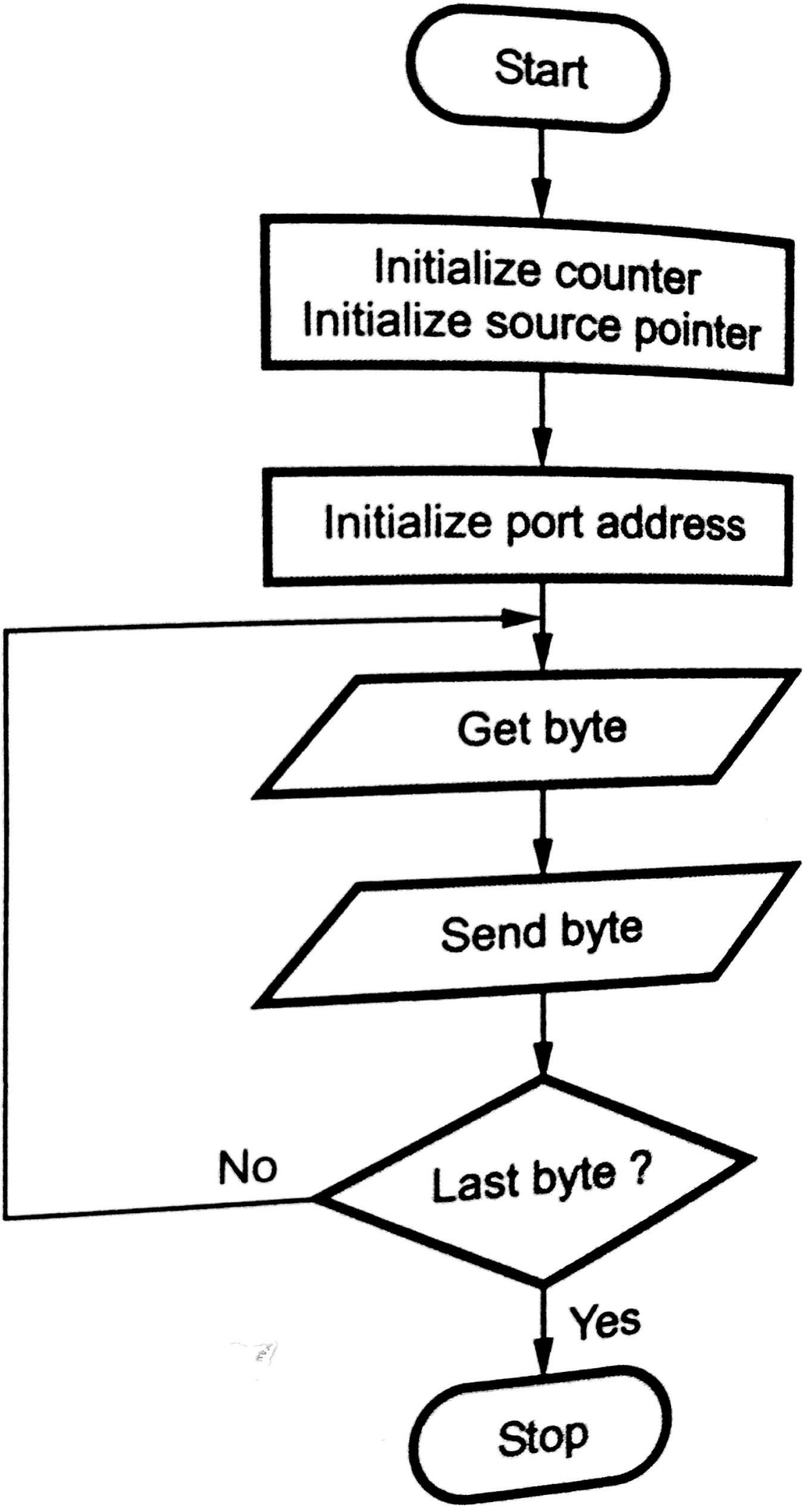
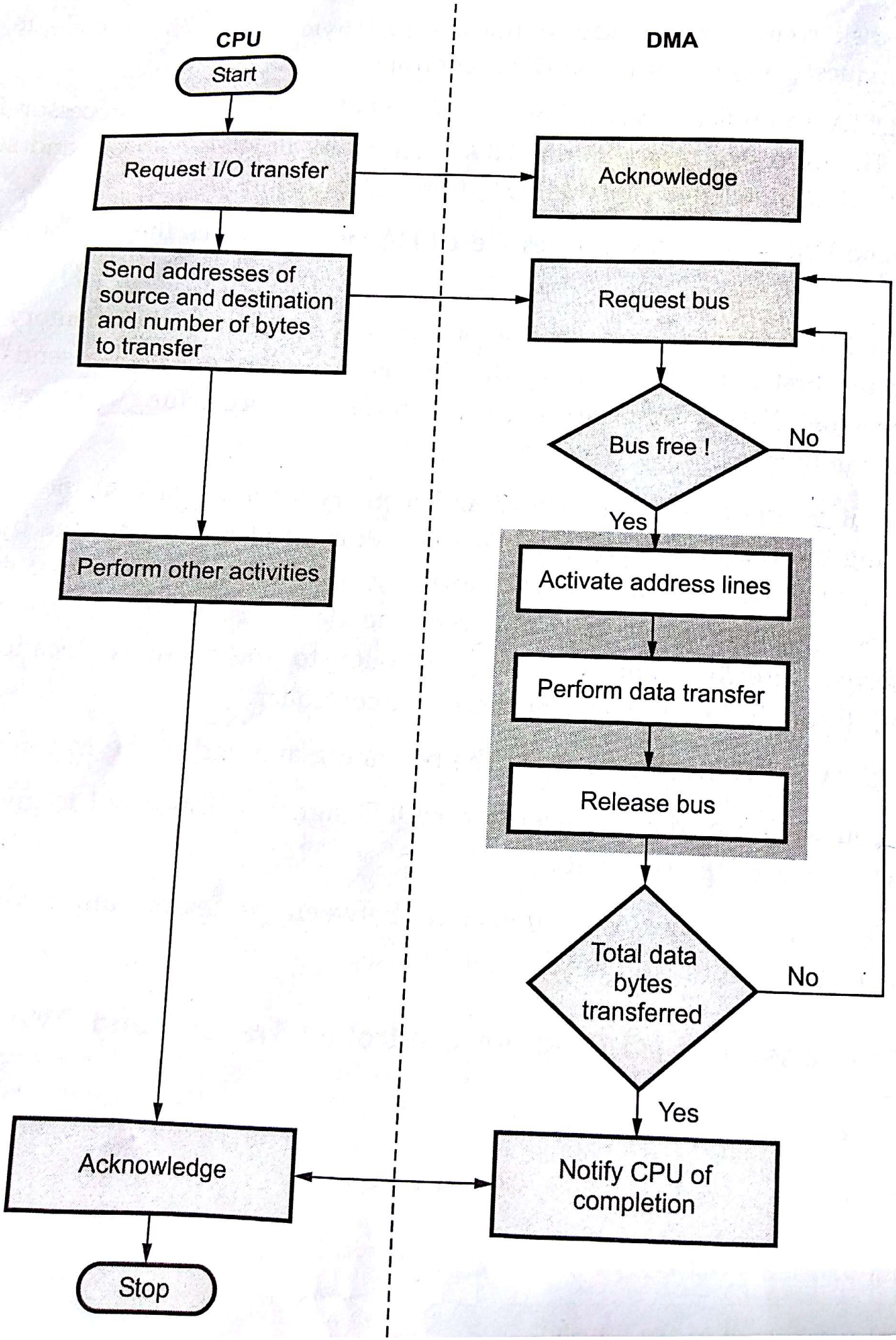
ution fetch, decode and execute




CPU
DMA
Start
Request I/O transfer
Acknowledge
Send addresses of source and destination and number of bytes to transfer
Request bus
Bus free !
No
Yes
Perform other activities
Activate address lines
Perform data transfer
Release bus
Total data bytes transferred
No
Yes
Acknowledge
Notify CPU of completion
Stop

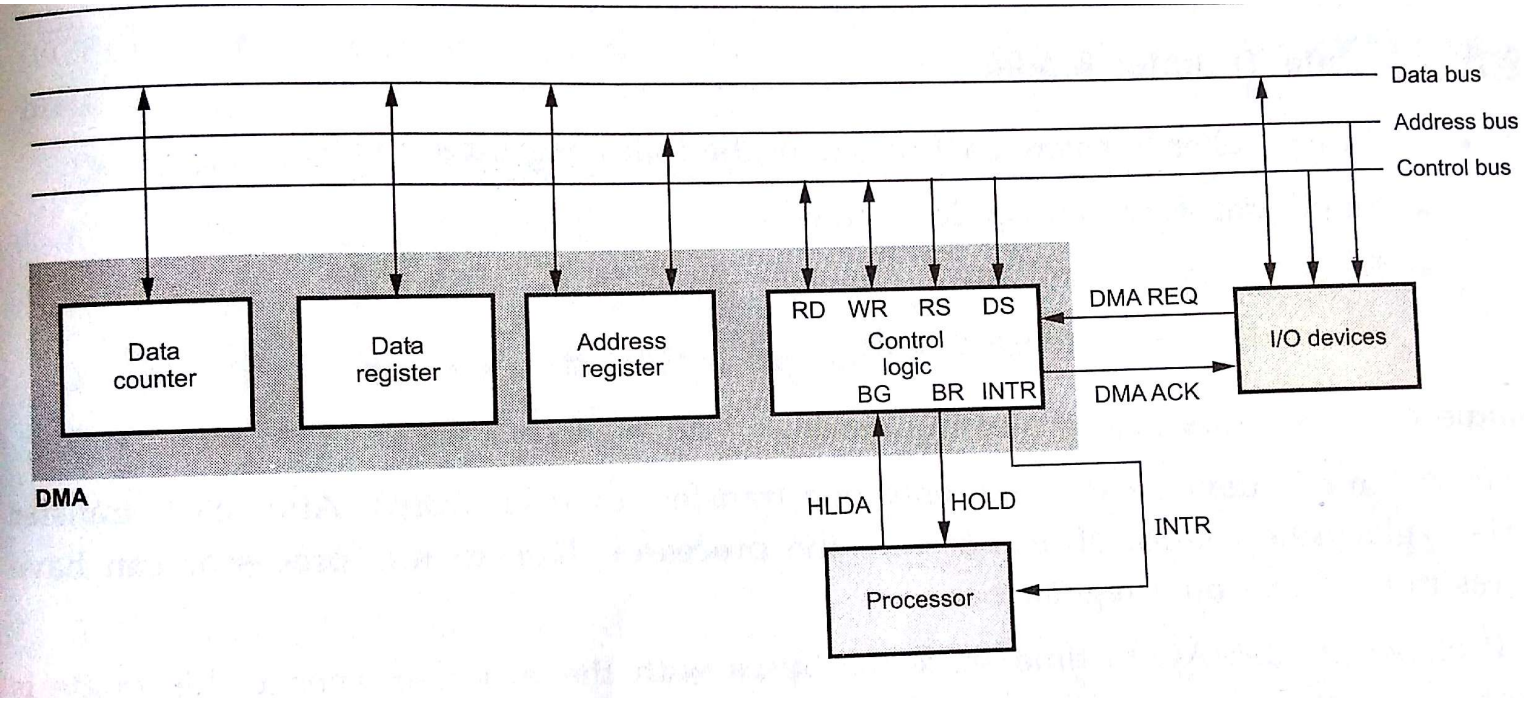

Data bus
Address bus
Control bus
Data counter
Data register
Address register
RD WR RS DS
Control logic
BG BR INTR
DMA REQ
DMA ACK
I/O devices
DMA
HLDA
HOLD
INTR
Processor

Fig. 5.10.5 (a) Use of DMA controllers in a computer system

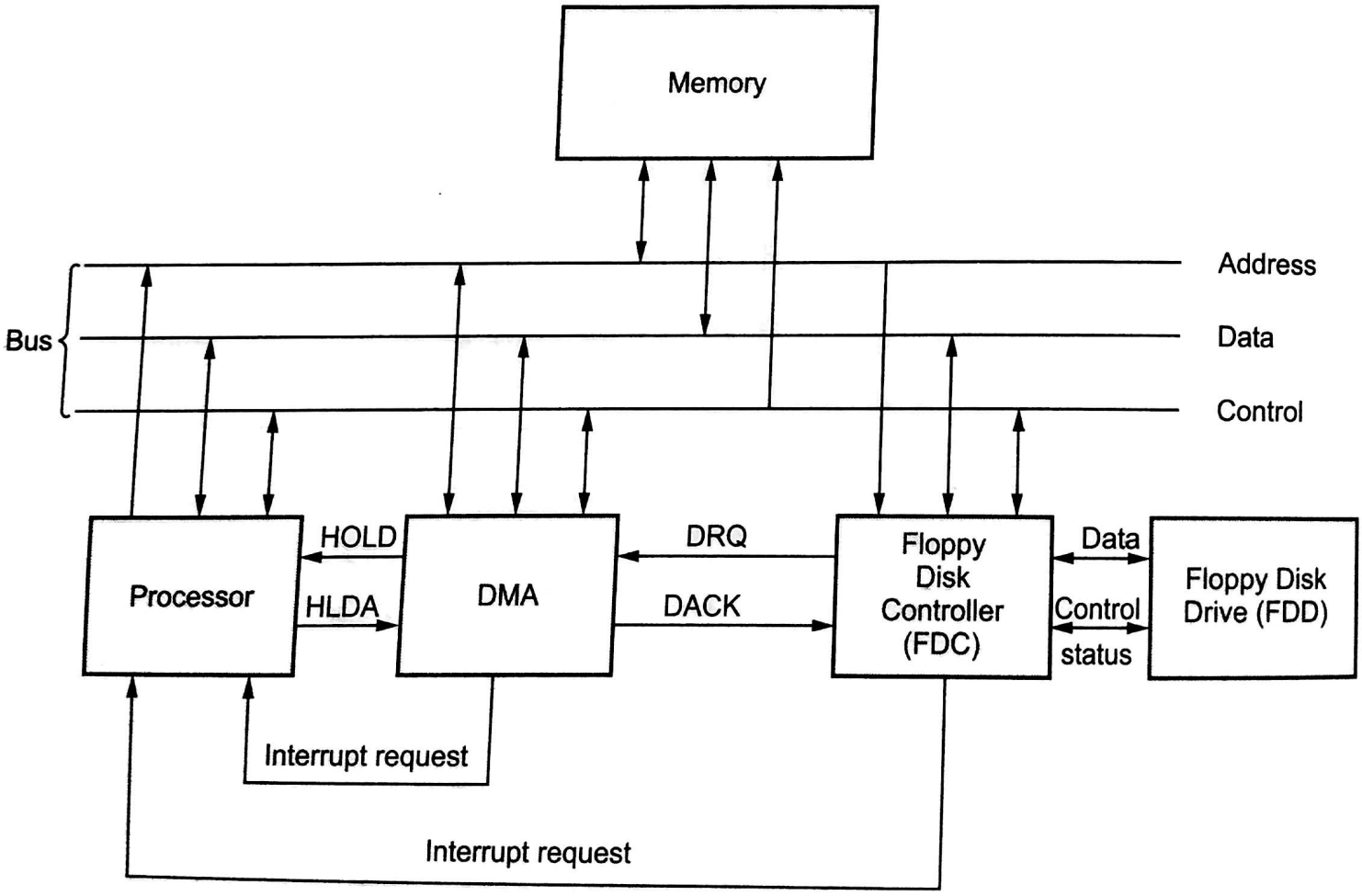


Fig. 5.10.5 (b)