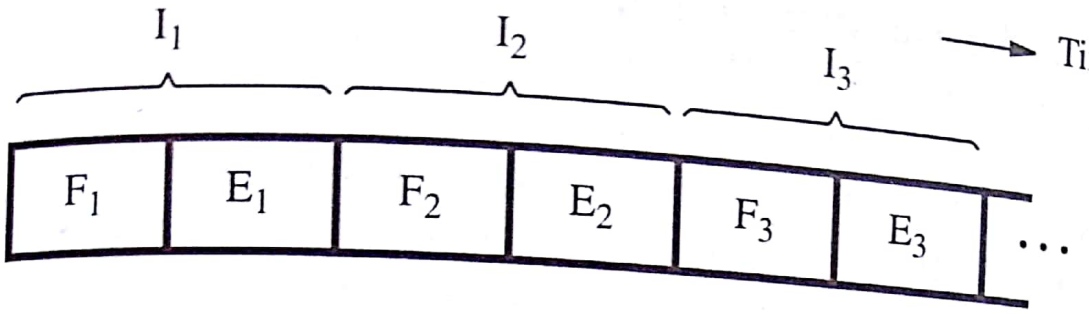
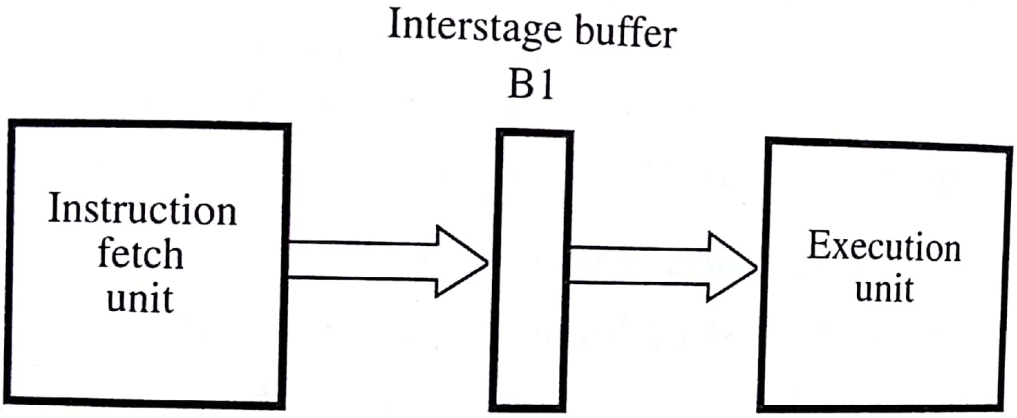
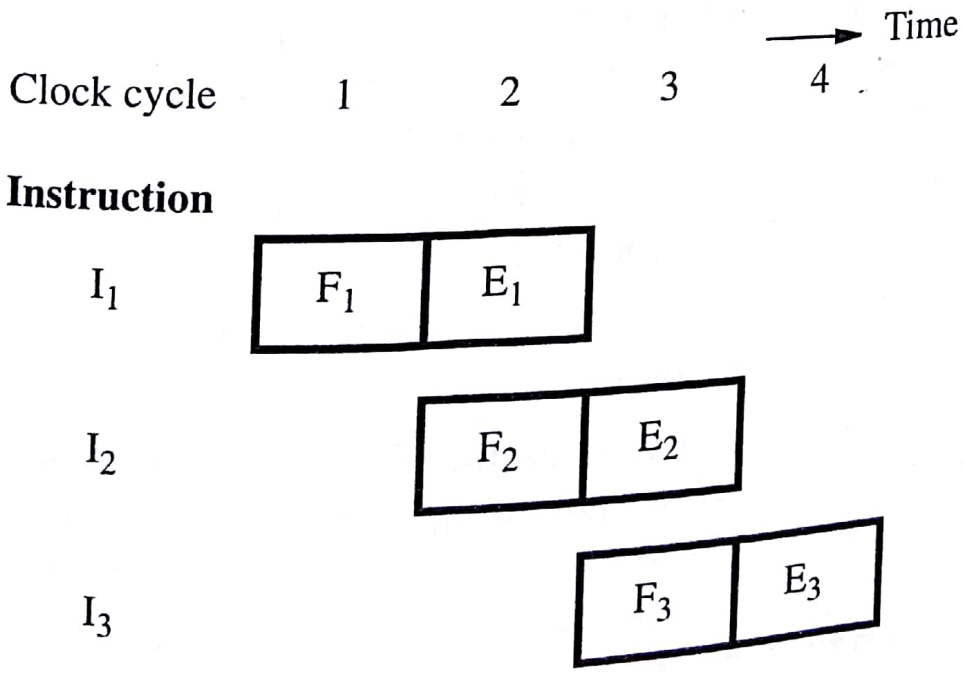


(a) Sequential execution



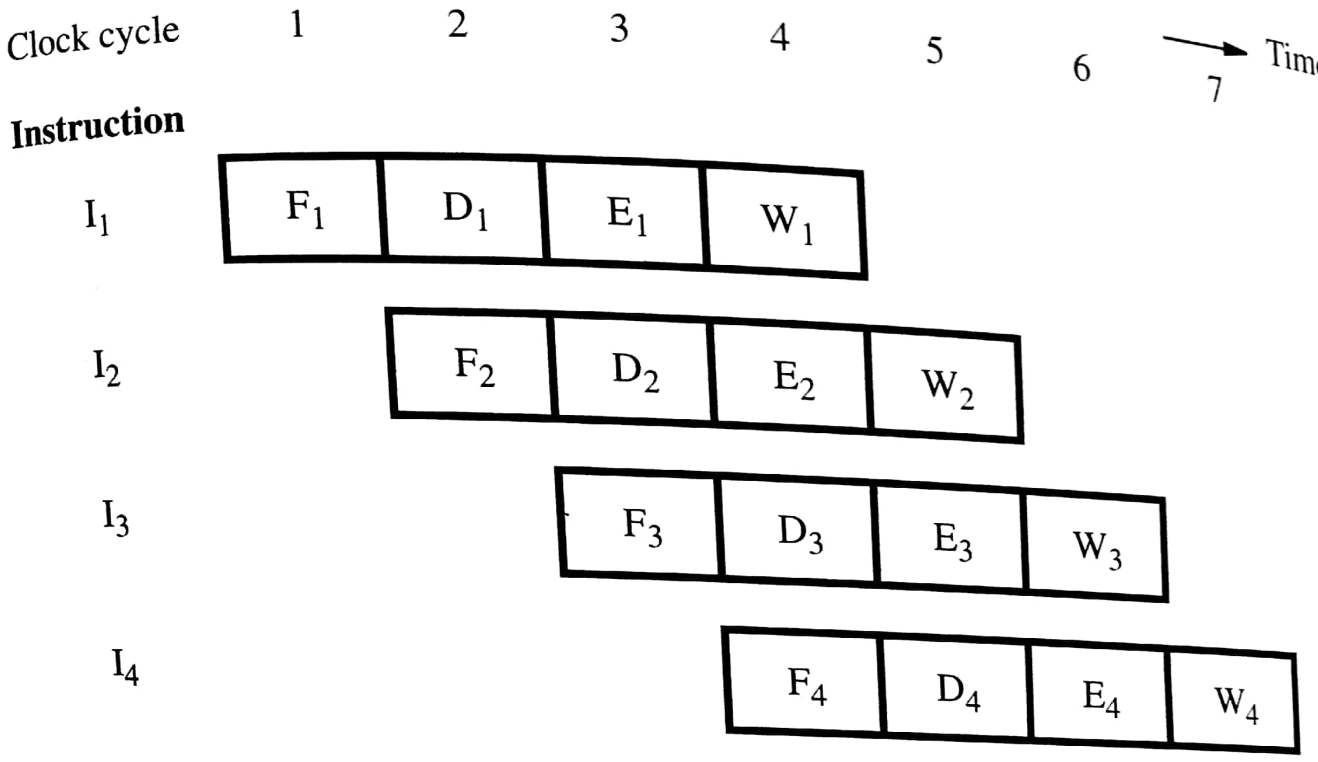
(b) Hardware organization



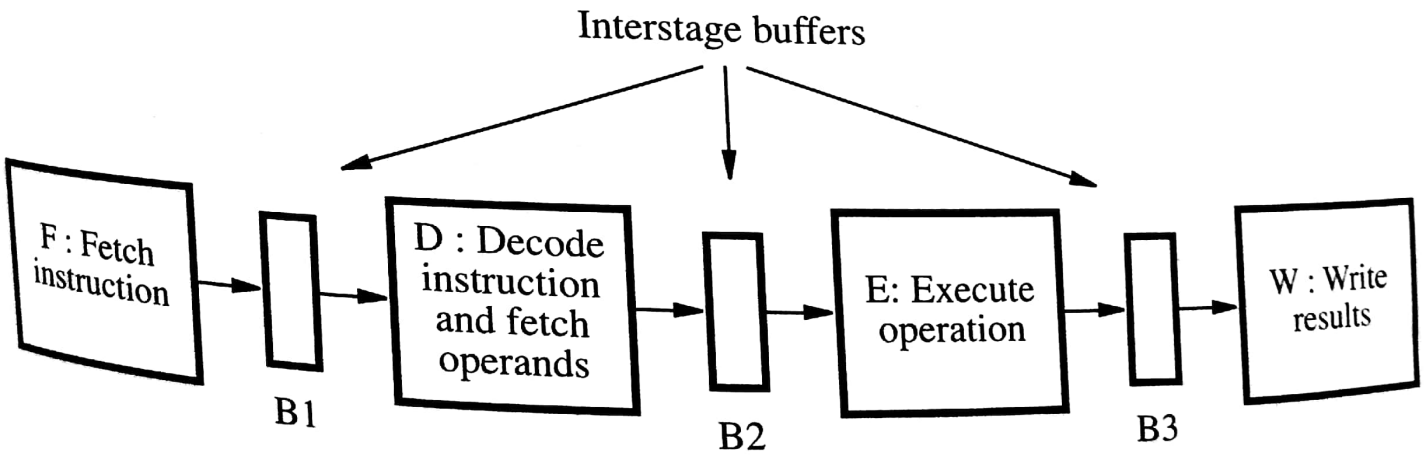
(c) Pipelined execution

Figure 8.1 Basic idea of instruction pipelining.

and



(a) Instruction execution divided into four steps



(b) Hardware organization

Figure 8.2 A 4-stage pipeline.

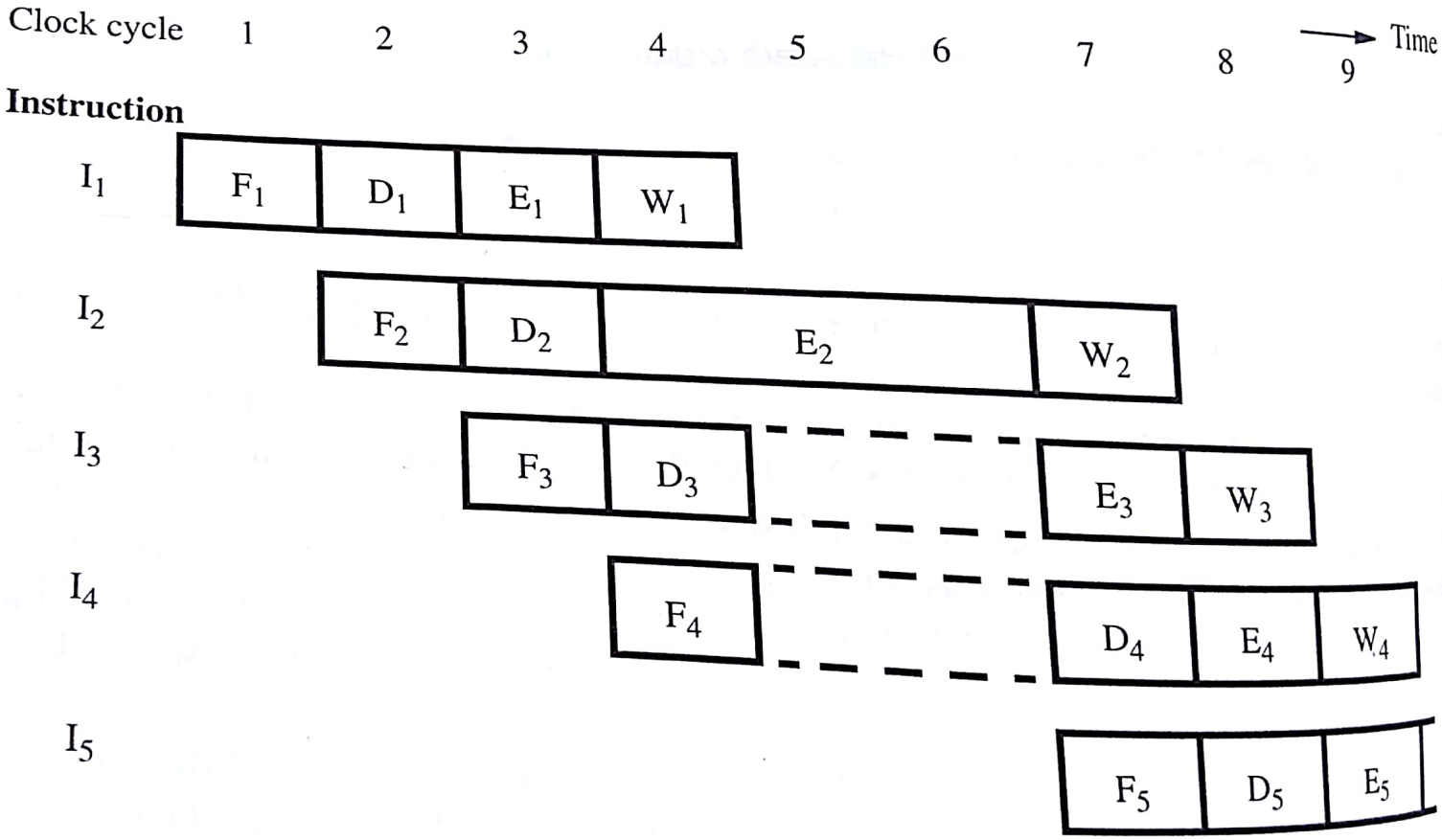


Figure 8.3 Effect of an execution operation taking more than one clock cycle.